CMS24AD2001

User Manual

24-bit Sigma-Delta ADC

Rev. 1.12

Index

1. Chip Function Description

The CMS24AD2001 is a high-precision and low-power analog-to-digital converter (ADC) chip. It supports one differential input channel, one built-in linear voltage regulator (LDO), temperature sensor and high-precision oscillator. The output capacity of LDO is 20 mA. The programmable gain amplifier (PGA) of CMS24AD2001 supports selectable gain options of 1, 2, 4, 8, 16, 32, 64, 128 and 256. The ADC output data rate(ODR) in the normal mode of CMS24AD2001 is optional: 2.5Hz-2.56KHz, and the default is 5Hz. The CMS24AD2001 employs 2-wire SPI serial interface SCLK, DRDYB/DOUT to communicate with external controllers.

The CMS24AD2001 can be configured by 2-wire SPI interface for different function such as channel selection, temperature sensing, PGA gain settings, ADC ODR settings, etc.

1.1 Features

- Built-in LDO
- Support single differential input
- Built-in oscillator
- Integrated temperature sensor
- Supports sleep mode
- 2-wire SPI interface, the maximum rate is 1.1MHz
- ADC features:
  - 24-bit no missing code
  - Optional PGA gain: 1, 2, 4, 8, 16, 32, 64, 128, 256
  - Optional ODR: 2.5Hz-2.56KHz
  - PGA = 128, ODR = 10Hz, SET_LDO = 00, the effective resolution is 20.6-bit
  - PGA = 128, ODR = 10Hz, SET_LDO = 00, the input referred noise is 30nVrms

1.2 Application

- Weigh scale
- Liquid/gas chemical analysis
- Instrumentation
- Industrial process control
- Sensor signal acquisition

1.3 Device Overview

The CMS24AD2001 is a high-precision and low-power Sigma-Delta ADC chip. It supports one differential input channel, one LDO, Sigma-Delta ADC and temperature sensor. The ADC employs Sigma-Delta modulator and realizes PGA amplifier through low-noise instrument amplifier structure. The gain can be selected as 1, 2, 4, 8, 16, 32, 64, 128 and 256. When PGA = 128 and ODR = 10Hz, the effective resolution can reach 20.6-bit.

The CMS24AD2001 has a built-in oscillator without external oscillator.

The CMS24AD2001 can be configured by 2-wire SPI interface SCLK, DRDYB/DOUT for different function such as temperature sensing, PGA gain settings, ADC ODR settings, etc.

The CMS24AD2001 supports sleep mode.

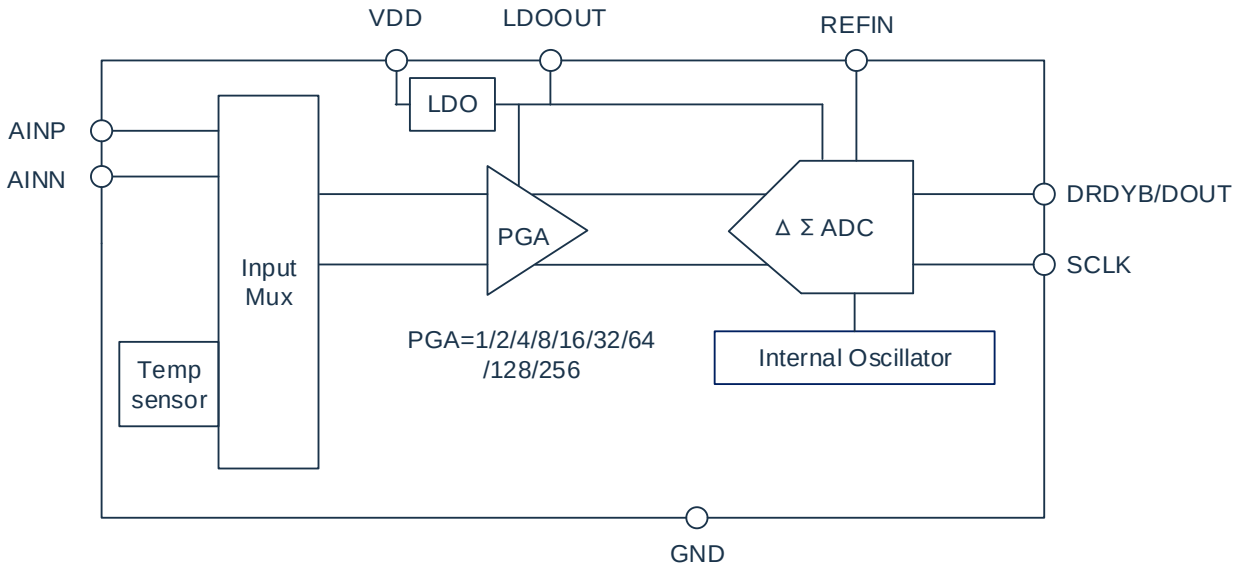


Figure 1-1: CMS24AD2001 Block Diagram

1.4 Absolute Maximum Ratings

Table 1-1: CMS24AD2001 Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Power Supply Voltage	VDD	-0.3	4.4	V
Digital Pin Input Voltage	-	-0.3	VDD+0.3	V
Operating Temperature Range	-	-40	85	℃

1.5 Electrical Characteristics – Digital

Table 1-2: CMS24AD2001 Digital Electrical Characteristics

Parameters	Min.	Typ.	Max.	Units	Condition
VIH	0.7xVDD	-	VDD+0.1	V	-
VIL	GND	-	0.3xVDD	V	-
VOH	VDD-0.4	-	VDD	V	-
VOL	GND	-	0.2xVDD	V	-
Serial SCLK Frequency	0.1	-	1.1	MHz	-

1.6 Electrical Characteristics – Analog

Table 1-3-a: CMS24AD2001 Analog Electrical Characteristics

Parameters	Min.	Typ.	Max.	Units	Condition
Analog Inputs					
Differential Input Range	-REFIN/PGA	-	REFIN/PGA	V	-
Common Mode Input Range	GND+0.75		VDD-1	V	-
Differential Input Impedance	-	250	-	Mohm	-
System Performance					
Resolution	-	24	-	bits	No missing code
ODR	2.5	5	2.56K	Hz	-
Settling Time	-	-	3	Conversion Cycle	Settled
Input Referred Noise		30	-	nVrms	PGA=128, 10Hz, LDO=3V
Effective Resolution	-	20.6	-	bits	PGA=128, 10Hz, LDO=3V
Offset Error	-	2.5	10	uV	PGA=64,128
Offset Error Drift	-	30	-	nV/℃	PGA=64,128
Gain Error	-	±1.5	-	%	PGA=64,128
Gain Error Drift	-	16	-	ppm/℃	PGA=64,128
Voltage Reference Input	0.5	LDOOUT	LDOOUT	V	-
Temperature Sensing	-	±3	-	℃	-
Bandgap Reference Voltage	-	1.24	-	V	VDD=3.3V
LDO					
Output Voltage	-	3.07	-	V	SET_LDO[1:0]=00
	-	2.66	-	V	SET_LDO[1:0]=10
Load Capacity	-	20	-	mA	VDD=3.3V
Power Supply					
Power Supply Voltage	2.5	3.3	4.4	V	-
Supply Current (Normal Mode)	-	1.68	-	mA	PGA=128
	-	0.83	-	mA	PGA=2
Supply Current (Sleep Mode)	-	50	-	nA	-

Table 1-3-b shows the effective resolution of CMS24AD2001 under different ODR and PGA gains. Test conditions: the power supply voltage is 3.3V, the temperature is 27℃, the LDO is set as 3V output, the reference voltage is LDO output voltage, the common mode input voltage is 0.5 times LDO output voltage, the differential input voltage is 0 V, and the total amount of data under each setting of a single chip is 1000.

Effective Resolution=Log2 (2*REFIN /RMS_Noise)

Table 1-3-b: CMS24AD2001 Effective Resolution

Effective Resolution	FADC	656K (FADC=1)							
	OSR(Over Sample Rate)	64	128	256	1024	4096	8192	16384	32768
	ODR (Hz)	2560	1280	640	160	40.0	20.0	10	5
PGA Gain	2 (0000b)	15.0	17.4	18.6	19.8	20.7	21.2	21.7	22.1
	4 (0001b)	15.0	17.2	18.5	19.6	20.5	21.2	21.7	22.1
	8 (0011b)	14.9	17.3	18.4	19.5	20.5	21.0	21.6	22.1
	16 (0100b)	15.1	17.3	18.4	19.5	20.5	21.2	21.6	22.1
	32 (0101b)	15.0	17.1	18.2	19.3	20.3	20.8	21.4	21.8
	64 (0110b)	15.1	17.2	18.1	19.3	20.3	20.8	21.3	21.8
	128 (0111b)	14.9	16.7	17.6	18.7	19.7	20.1	20.6	21.1
	256 (1000b)	14.8	16.0	16.7	17.8	18.8	19.2	19.8	20.3

1.7 Pin Description

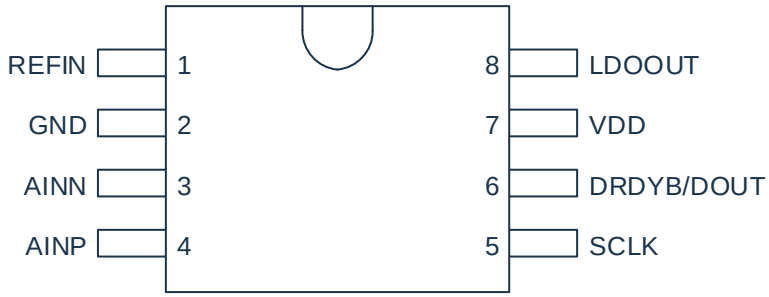


Table 1-4: SOP8 Pin Description

Pin No	Name	Analog/Digital Input/Output	Description
1	REFIN	AI	Voltage Reference Input, shall not be higher than LDOOUT voltage
2	GND	P	Ground
3	AINN	AI	Negative Analog Input
4	AINP	AI	Positive Analog Input
5	SCLK	DI	SPI Clock Input
6	DRDYB/DOUT	DI/DO	SPI Data Input/output
7	VDD	P	Power Supply
8	LDOOUT	P	Internal LDO output, external capacitance 1uF(Min) is required

2. System Description

2.1 LDO

The built-in LDO of CMS24AD2001 can supply power to the on-chip analog module, at the same time, it can provide 20 mA current to the off-chip circuit. LDOOUT pin shall be connected externally with a capacitor at least 1uF. Different LDO output voltages can be configured by setting SEL_ LDO [1:0], such as 2.4V, 2.6V, 3V and 3.3V. LDO can also be configured to work in switch mode or linear voltage regulator mode by setting BYPASSLDO. When the chip enters sleep mode, LDO output drops to 0 V.

2.2 Analog Inputs

CMS24AD2001 has one ADC integrated with one differential input channel. The analog input sources include 1 external differential analog inputs AINP/AINN, and one internal temperature sensor output. The internal multiplexer is used to select different analog input sources. The multiplexer is configured by CH_SEL[2:0].

2.3 Temperature Sensor

CMS24AD2001 has an internal temperature sensor. It is recommended to use the configuration with PGA gain = 8 and ADC ODR = 640Hz. One-point temperature calibration is recommended to improve accuracy.

Here is the calibration method: When ambient temperature becomes stable, record the temperature A with an accurate thermometer and record the temperature code Ya from CMS24AD2001. Then other real temperature B can be calculated by B= Yb*(273.15+A)/Ya-273.15. The unit of temperature A is Celsius. Ya is the temperature code corresponding to temperature A. Yb is the temperature code corresponding to temperature B.

For applications where the reference voltage may change (such as ratio metric measurement, the absolute value of the reference voltage is not important), you can choose to indirectly measure the real-time reference voltage by measuring BG, and then calculate the real-time temperature.

2.4 Low Noise Programmable Gain Amplifier

CMS24AD2001 employs a high performance low noise PGA with chopper technique, which is connected with the differential output of bridge sensor. PGA_SEL[3:0] is used to configure different gain such as 2, 4, 8, 16, 32, 64, 128 and 256. When PGA=2, 4, 8, the first stage amplifier of the PGA is disabled to save power. The absolute/common mode input voltage of the PGA is limited to be within GND+0.75V and VDD-1V, otherwise the performance would be deteriorated. When bypass PGA , the analog input is connected directly to ADC, the gain is 1.

2.5 ADC Clock, Output Data Rate

CMS24AD2001 has a built-in oscillator to provide the clock required by the system. 328KHz or 656KHz can be selected through FADC. The ODR of ADC can be configured through FADC and OSR [2:0]. It is recommended to operate the chip in 656KHz.

Table 2-1: Clock, ODR

FADC	OSR[2:0]	ODR	ADC Clock
0	111	2.5Hz	328KHz
0	110	5Hz	328KHz
0	101	10Hz	328KHz
0	100	20Hz	328KHz
0	011	80Hz	328KHz
0	010	320Hz	328KHz
0	001	640Hz	328KHz
0	000	1.28KHz	328KHz
1	111	5Hz	656KHz
1	110	10Hz	656KHz
1	101	20Hz	656KHz
1	100	40Hz	656KHz
1	011	160Hz	656KHz
1	010	640Hz	656KHz
1	001	1.28KHz	656KHz
1	000	2.56KHz	656KHz

2.6 Power On Reset and Sleep

When the chip is powered on, the built-in power-on reset(POR) circuit will generate a reset signal to reset the chip automatically. When SCLK toggles from low to high level and keeps high state for more than 100us, the CMS24AD2001 enters sleep mode, and the power consumption is less than 50na. When SCLK returns to low level, the chip returns to normal mode. The sleep mode does not change any internal registers, thus no reconfiguration is required when chip goes back to normal mode.

As shown in figure below, t00 represents hold-on time of SCLK high level before entering sleep mode, which needs to be larger than 100us; t01 represents hold-on time of SCLK low level before the chip returning to normal mode, which needs to be larger than 10us.

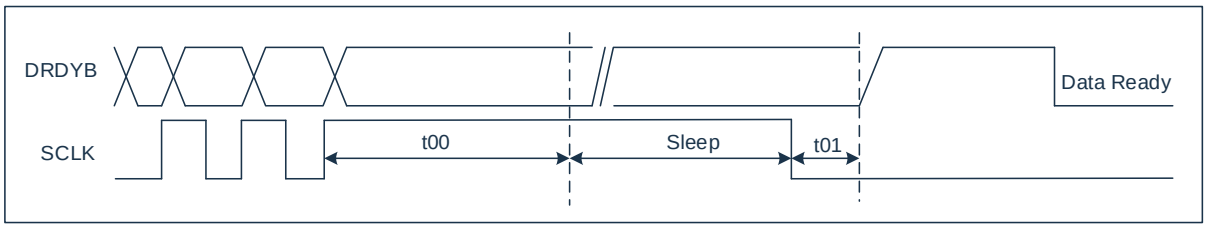


Figure 2-1: Sleep Mode Timing

2.7 Settling Time

The settling time of CMS24AD2001 is 3 conversion cylcles.

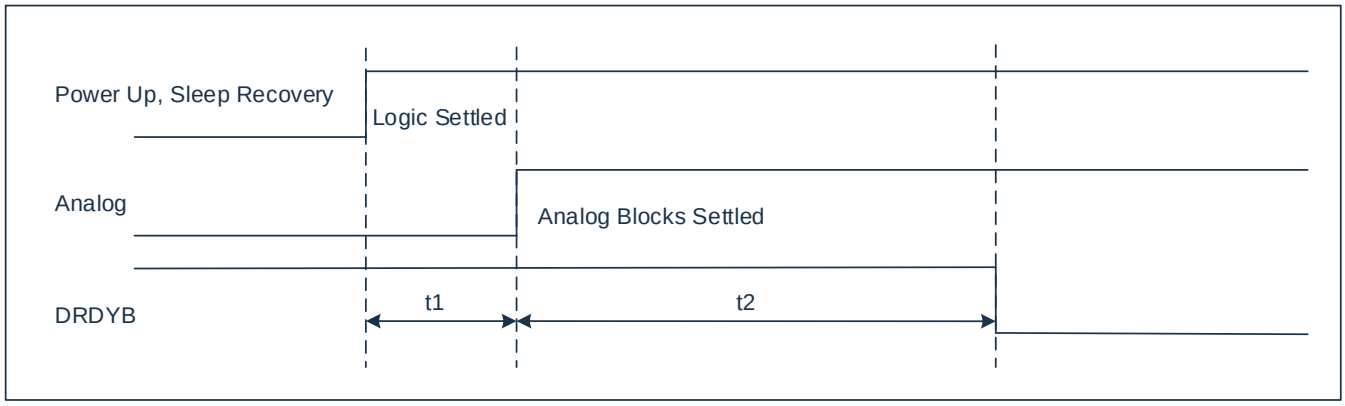


Figure 2-2: Data Settling Time Type-1

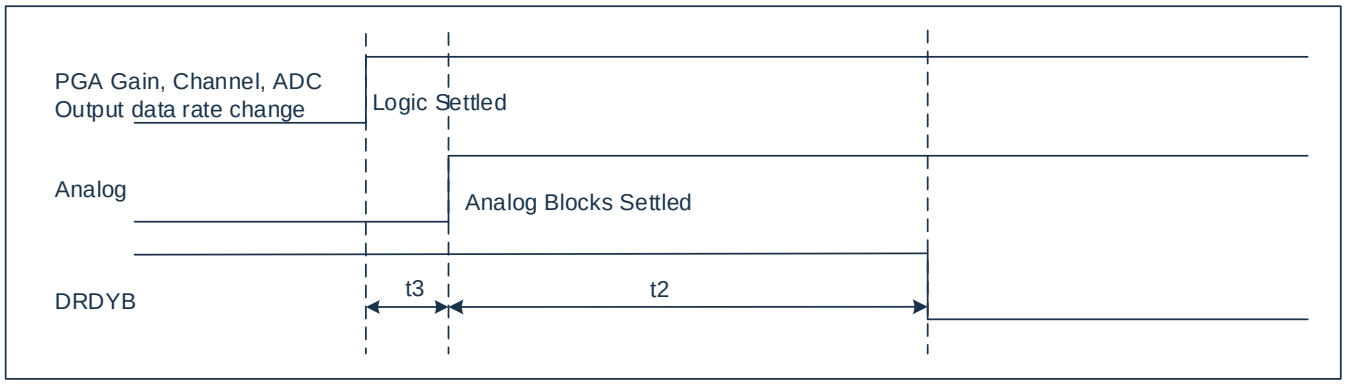


Figure 2-3: Data Settling Time Type-2

Table 2-2: Setting Time

Parameters	Description	Min.	Typ.	Max.	Units
Settling Time					
t1	Power-up, Recovery Time from Sleep Mode	-	0.4	-	ms
t2	Data Settling Time	-	3	-	Conversion cycle
t3	Time to get stabilized after PGA Gain, Channel, ADC ODR switching	-	0.8	-	us

2.8 SPI Serial Interface

The CMS24AD2001 employs 2-wire SPI serial interface SCLK, DRDYB/DOUT to communicate with external controllers.

2.8.1 Digital Output Codes

The output data of CMS24AD2001 is a 24-bit digital output code. Bit 23 to Bit 0 represents the output code in 24-bit binary two's complement. Bit 23 is the sign bit and is logic '0' when the differential analog input is positive and logic '1' when the differential analog input is negative. From Bit 22 to Bit 0, the output code is given MSB first (MSB is Bit 22 and LSB is Bit 0). The relationship between input voltage and output code is shown in Table 2-3.

Table 2-3: Data Output Codes Format

Analog Input Voltage	Digital Output Code																								Decimal Code	Hex Code
	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		B[23:0]
Vref-1LSB	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	8388607	7FFFFF
2LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2	000002
1LSB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	000001
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	000000
-1LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	FFFFFF
-2LSB	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	-2	FFFFFE
-Vref	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-8388608	800000

2.8.2 Data Ready, Data Output, Data Input（DRDYB/DOUT）

DRDYB/DOUT is the digital input/output pin of the device and serves four purposes. First, it indicates when a conversion is completed by going active-low, acting as a ready flag. Second, on the first rising edge of SCLK after data ready, this pin begins outputting ADC data from MSB to LSB. After the 24th SCLK rising edge, the device already outputs all ADC code. Afterwards, if SCLK stops after its falling edge, DRDYB/DOUT will keep the Bit 0 and then return to high until the next conversion completes. Later, DRDYB/DOUT will go active-low after the new conversion is completed, it indicates new data can be read out. Third, when 25th and 26th SCLK arrive, DRDYB/DOUT will output the written-flag of registers. Fourth, DRDYB/DOUT also acts as read/write pin for internal registers. 46 SCLKS needs to be send by SPI when it needs to write or read register. According to the command words input by DRDYB/DOUT, it can determine whether to write or read register.

2.8.3 Serial Input Clock（SCLK）

The serial clock input SCLK is a digital pin. This signal shall be a clean signal. Burr or slow rising edge may lead to reading wrong data or entering the wrong state by mistake. Therefore, the rise and fall time of SCLK shall be less than 50ns.

2.8.4 Data Retrieval

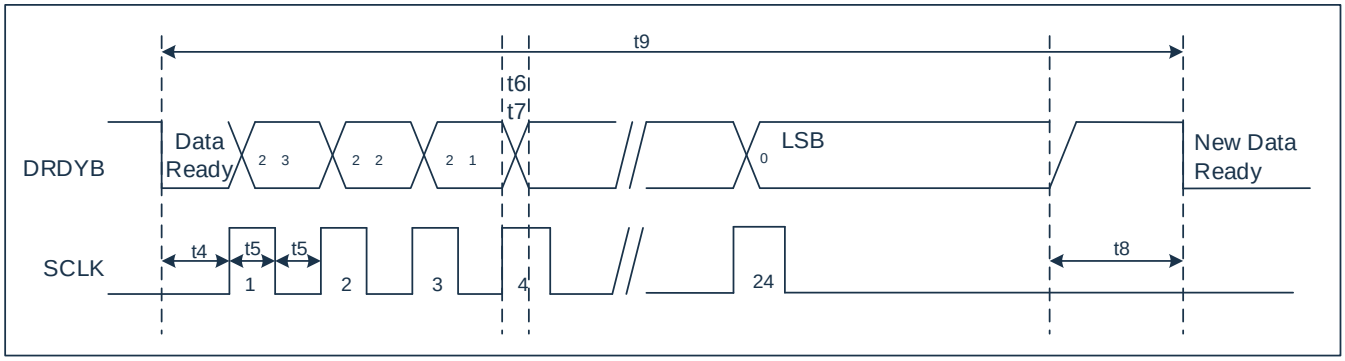


Figure 2-4: Data Retrieval Timing type-1

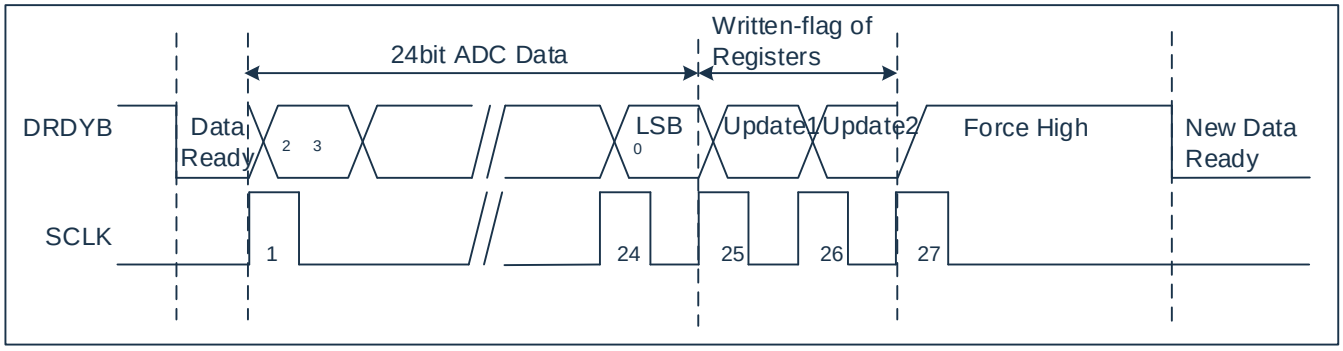


Figure 2-5: Data Retrieval Timing type-2

CMS24AD2001 works continuously to convert analog input signals. DRDYB/DOUT's toggling from high to low indicate the data is ready to accept. After the 1th SCLK rising edge, the Bit 23 of the output can be read out. After the 24th SCLK rising edge, all 24 bit data can be read out. Afterwards, if SCLK stops after its falling edge, DRDYB/DOUT will keep the Bit 0(LSB) and then return to high until the next conversion completes. The timing is shown in is shown in Figure 2-4.

If 25th and 25th SCLK arrive, DRDYB/DOUT will output the written-flag of registers during the 25th SCLK and output 0 during the 26th SCLK. If one of those registers have been written during last conversion, the written-flag will be 1. Otherwise, the output will be 0. After the 27th SCLK, DRDYB/DOUT will be pulled to high. If there is no more SCLK, DRDYB/DOUT keeps high until the next conversion is completed. Figure 2-5 shows the timing diagram.

Table 2-4: Timing of Data Retrieval

Parameters	Description	Min.	Typ.	Max.	Units
t4	DRDYB/DOUT falling edge to first SCLK rising edge	-	2	-	ns
t5	SCLK positive or negative pulse width	455	-	-	ns
t6	SCLK rising edge to new data bit valid (propagation delay)	455	-	-	ns
t7	SCLK rising edge to previous data bit valid (hold time)	-	-	455	ns
t8	Data update. It is not allowed to read previous data	-	26	-	us
t9	Conversion time, 10Hz	-	100	-	ms
	Conversion time, 40Hz	-	25	-	ms
	Conversion time, 640Hz	-	1.5625	-	ms

2.8.5 Register Configuration

CMS24AD2001 configures or reads internal registers by SCLK and DRDYB/DOUT. The register configuration timing is shown in Figure 2-6.

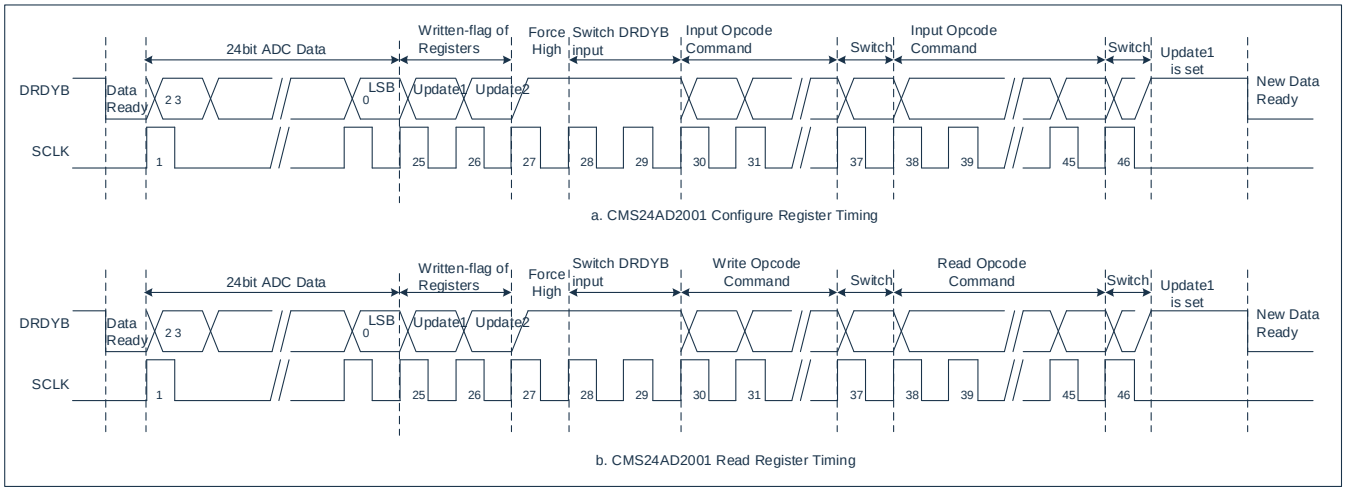


Figure 2-6: Register Configuration Timing Type-3

Here is configuration procedures after data ready, i.e. DRDYB/DOUT toggles from high to low:

1) From 1st to 24th SCLK. DRDYB/DOUT outputs 24-bit ADC data. The following steps can be ignored if no register configuration is required.
2) From 25th to 26th SCLK. DRDYB/DOUT outputs the written-flag of registers during the 25th SCLK and output 0 during the 26th SCLK.
3) During 27th SCLK. DRDYB/DOUT is pulled to high automatically.
4) From 28th to 29th SCLK. DRDYB/DOUT pin is switched to input mode.
5) From 30th to 36th SCLK. The opcode command is input or read out through DRDYB/DOUT with MSB first and LSB last.
6) During 37th SCLK. DRDYB/DOUT pin function maybe changed. If opcode indicates to read a register, DRDYB/DOUT becomes output pin. If opcode indicates to configure a register, the DRDYB/DOUT remains as input pin.
7) From 38th to 45th SCLK. Configure or read register data. MSB first and LSB last.
8) During 46th SCLK. DRDYB/DOUT pin is switched to output mode and holds high. Register bits Update1/ update2 is set or reset.

2.8.6 SPI Opcode Command

CMS24AD2001 has 8 opcode command word with 7-bit length.

Table 2-5: SPI Opcode Command

Name	Opcode Command	Funtion	Remark
SDADCCON1	0x65	Write SDADCCON1	Configured by 2-wire SPI
	0x56	Read SDADCCON1	Configured by 2-wire SPI
SDADCCON2	0x69	Write SDADCCON2	Configured by 2-wire SPI
	0x5A	Read SDADCCON2	Configured by 2-wire SPI
SDADCCON3	0x6D	Write SDADCCON3	Configured by 2-wire SPI
	0x5E	Read SDADCCON3	Configured by 2-wire SPI
SDADCCON4	0x61	Write SDADCCON4	Configured by 2-wire SPI
	0x52	Read SDADCCON4	Configured by 2-wire SPI

2.8.7 Notes for SPI Communication

As described above, CMS24AD2001 has three different data retrieval or register configuration timing.

1) Type-1: Retrieve 24-bit ADC data.
2) Type-2: Retrieve 24-bit ADC data and 2-bit written-flag of registers.
3) Type-3: Retrieve 24-bit ADC data, 2-bit written-flag and read or write internal registers.

Notes:

1) The data read out is the result of the last ADC conversion before sending the timing sequence.
2) Judge that DRDYB/DOUT toggles from high to low before sending clock.
3) When sending any timing sequence, the time from DRDYB/DOUT falling edge to the completion of all data transmission shall be less than one conversion time (that is, the timing sequence is sent between two falling edges), otherwise DRDYB will be abnormal and can be recovered only after entering sleep mode.

2.9 Associated Register

2.9.1 Sigma-Delta ADC Control Register 1

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SDADCCON1	SET_LDO_1	SET_LDO_0	OSR_2	OSR_1	--	PGA_SEL2	PGA_SEL1	PGA_SEL0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	1	1	0	1	1	0

Bit7~Bit6 SET_LDO<1:0>: LDO output voltage control
00= 3V
01= 2.4V
10= 2.6V
11= 3.3V

Bit5~Bit4 OSR<2:1>: OSR settings (Conversion rate related)
000= 64
001= 128
010= 256
011= 1024
100= 4096
101= 8192
110= 16384
111= 32768

Bit3 --: Reserved, must be 0

Bit2~Bit0 PGA_SEL<2:0>: PGA gain
000= 2
001= 4
010= 8
011= 16
100= 32
101= 64
110= 128
111= 256

2.9.2 Sigma-Delta ADC Control Register 2

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SDADCCON2	CHSEL2	CHSEL1	SHSEL0	LPWR	FADC	OSR_0	ENCHOPB	FCHOP_ADC
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	1	0	0	0	0

Bit7~Bit5 CHSEL<2:0>: Channel selection
000= Channel-1
001= Channel-1 positive and negative switching (system chopper)
010= Temperature sensor
011= Short inputs
100= Channel-1 connect directly to ADC and bypass PGA
101= Channel-1 connect directly to ADC and bypass PGA
110= BG
111= Short inputs and connect directly to ADC

Bit4 LPWR: Power consumption selection
0= Lowest power consumption
1= Normal power consumption

Bit3 FADC: Sigma-Delta ADC system clock
0= 328KHz
1= 656KHz(recommended)

Bit2 OSR_0: OSR LSB

Bit1 ENCHOPB: ADC chopper control
0= Enable chopper function
1= Disable chopper function

Bit0 FCHOP_ADC: ADC chopper frequency division control
0= Divided by 16
1= Divided by 32

2.9.3 Sigma-Delta ADC Control Register 3

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SDADCCON3	--	--	--	--	--	BYPASSLDO	OCP_DIS_LDO	--
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	0	1	0	0	0

Bit7~Bit4 --: Reserved, must be 1000

Bit3 --: Reserved, must be 1

Bit2 BYPASSLDO: LDO bypass control
0= LDO output
1= Bypass LDO and output VDD

Bit1 OCP_DIS_LDO: LDO output overcurrent protection enable control
0= Enable
1= Disable

Bit0 --: Reserved, must be 0

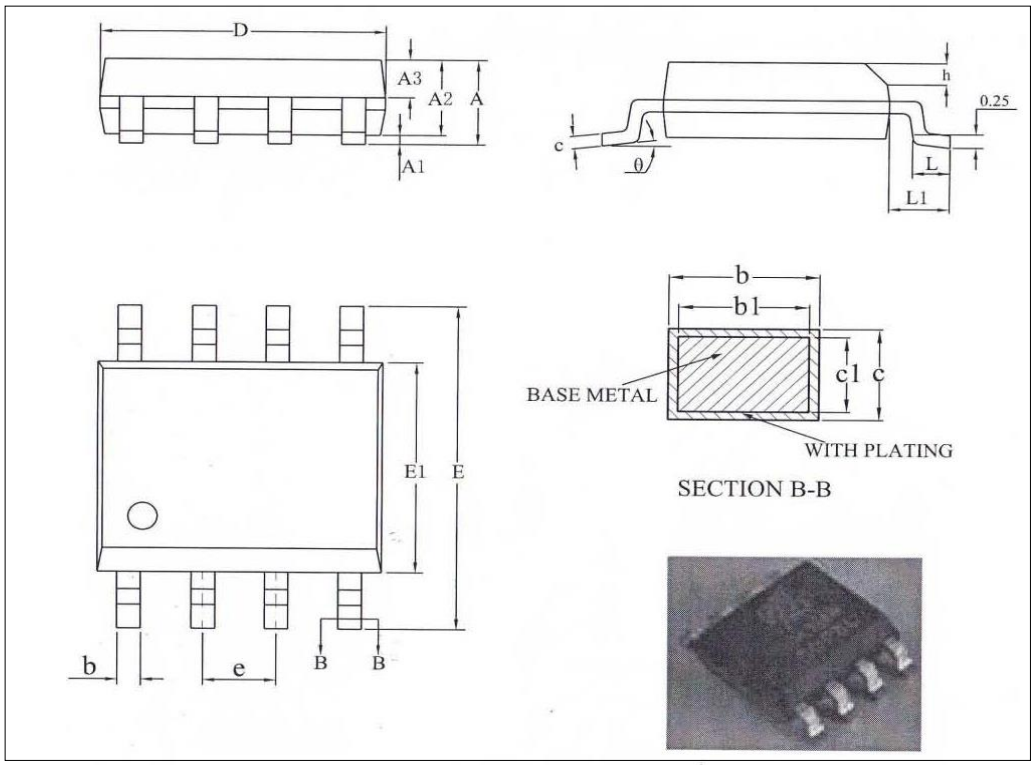
2.9.4 Sigma-Delta ADC Control Register 4

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SDADCCON4	--	--	--	--	--	--	FCHOP_1	FCHOP_0
Read/write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	1	0	0	0	0	0	0	1

Bit7~Bit4 --: Reserved, must be 1000
Bit3~Bi2 --: Reserved, must be 00
Bit1~Bit0 FCHOP<1:0>: PGA chopper frequency division control
00= Divided by 4
01= Divided by 8
10= Divided by 16
11= Divided by 32

3. Package Dimensions

3.1 SOP8



Symbol	Millimeter		
	Min	Nom	Max
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.5	-	0.80
L1	1.05REF		
θ	0	-	8°

4. Version Revision Description

Revision	Date	Modify content
V1.00	Sep 2021	Initial version
V1.10	Dec 2021	AD2001 only support single channel, deleted dual channel related content
V1.11	Jan 2022	Refined some register description…etc.
V1.12	Mar 2022	Revise some expressions